JPRS-JST-91-011
14 MARCH 1991

JPRS Report

Science & Technology

Japan

TOKAI REGIONAL SEMINAR ON HIGH TEMPERATURE SUPERCONDUCTIVITY

JPRS-JST-91-011
14 MARCH 1991

SCIENCE & TECHNOLOGY
JAPAN

TOKAI REGIONAL SEMINAR ON HIGH TEMPERATURE SUPERCONDUCTIVITY

916C0001 Tokyo TOKAI CHIKU KO NO CHODENDO KENKYU HAPPYOKAI in Japanese
17 Jul 90 pp 1-47

[Selected papers presented at the Third Tokai Regional Seminar on High Temperature Superconductivity Research held 17 Jul 90 in Nagoya, sponsored by the Industrial Science Research Institute of Nagoya and the Tokai Branch of the Japan Society of Applied Physics]

CONTENTS

Current Status, Outlook for Josephson Computer R&D

916C0001A Tokyo TOKAI CHIKU KO ON CHODENDO KENKYU HAPPYOKAI in Japanese
17 Jul 90 pp 1-9

[Article by Susumu Takada, Electronic Device Department, Electronic Technology Research Laboratory]

[Text] **1. Preface**

Josephson junction devices carry out ultrahigh-speed switching operations using only several microwatts of power within several picoseconds. Josephson computers with Josephson junction devices are, therefore, expected to calculate with high efficiency. In cryogenic environments, superconducting electrons tunnel through an extremely thin film insulator. Such superconducting phenomenon is called "Josephson effect." Josephson junctions are electronic devices to which this Josephson effect is applied and operate completely differently from conventional switching devices. Josephson junction devices operate on electric power at several microwatts, greatly reducing the production of heat in integrated circuits and thereby achieving highly dense integrations. Thus, ultrahigh-performance digital systems are expected to be developed. Integrated circuits using Josephson devices allow electric wiring and connections between devices to be carried out using superconductors. Transmission of ultrahigh-speed signals (which feature superconducting lines) with low loss and high quality, therefore, is possible.

Technology to integrate Josephson junction devices whose electrodes are made of metal group superconducting materials--that is, niobium (Nb) and niobium nitride (NbN)--has recently been developed. As a result, Josephson integrated circuits stably operate with high reliability. Therefore, Nb-based Josephson integrated circuit research was promoted mainly by a Japanese research group and has made marked progress, coupled with the large-scale project promotion policy of the Ministry of International Trade and Industry (MITI). This research includes the development of Josephson large-scale integrated (LSI) circuits, which lays emphasis on logic circuits, trial manufacture of Josephson processors, and development of Josephson random access memory (RAM) chips.

On the basis of the Josephson computer technology research to date, Electronic Technology Research Laboratory has recently developed a Josephson ETL-JCI

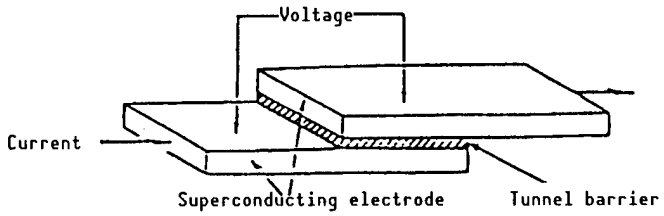
computer in which four Josephson LSI chips (each provided with functions such as read only memory (ROM) for operation, sequence control, instruction programs, and RAM for data storing) are combined with each other. This computer has for the first time verified computer operations by combining logic circuits with memory circuits. This report, therefore, describes the current status of and outlook for Josephson computer R&D, while reviewing the course of the Josephson integrated circuit research and the results of ETL-JCI research.

2. Research on Josephson Integrated Circuits

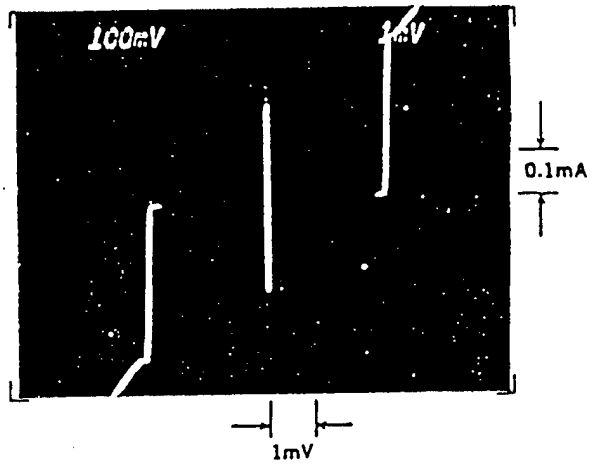
Josephson junction devices are based on the principles of the Josephson effect theoretically predicted by B.D. Josephson in England in 1962. Initial research on using these devices as switching devices in computer circuits was carried out in the United States by IBM W.J. Research Center and Bell Research Institute. Later, Josephson computer technology was researched positively at various research laboratories, ranging from superconducting materials used as Josephson junction device electrodes, tunnel barrier layers, Josephson logic devices, and integrated circuits to systems. In 1983, IBM stopped the Josephson computer project. Since then, Josephson computer technology research has been promoted by Japanese research laboratories, emphasizing large-scale project research conducted by the Agency of Industrial Science and Technology of MITI.

Figure 1(A) shows a schematic configuration of a Josephson junction device. It has a structure in which a thin-insulation tunnel barrier is sandwiched by two superconducting electrodes. When an electric current is applied to both electrodes via the tunnel barrier, the electric current flows between the upper and lower electrodes through the barrier during the superconducting state (zero electric resistance) as if there were no tunnel barriers. When the flow of electric current exceeds the Josephson critical current, Josephson direct current cannot flow through the barrier, and an electric resistance occurs between the electrodes, thus switching to a "voltage" state. This state is shown in Figure 1(B). The axis of ordinates shows electric current that flows in the device while the axis of abscissas shows voltage generated by the device.

While an electric current flows in the device during the superconducting state, no voltage occurs in the device. When the flow of the electric current reaches more than the critical current value, a certain amount of voltage occurs. As the flow of the current is reduced, voltage decreases producing an hysteresis. Switching to the voltage state is carried out at an extremely high speed, that is, several picoseconds (10^{-12}). As Figure 1(B) shows, Josephson junction devices go into two states, that is, the "superconducting" state that does not generate voltage when a bias current not exceeding the critical current value is applied and the "voltage" state that generates voltage. These two states correspond to bit "0" and bit "1," respectively, and digital circuits can thereby be formed. Josephson junction devices are characterized by the fact that they can carry out switching operations with extremely little energy. Compared with semiconductors, Josephson junction devices generate a voltage of only several mV, even if the same amount of current is applied.



(A) Schematic configuration



(B) Current-voltage characteristics (axis of coordinates: 0.1 mA, axis of abscissas: 0.1 mV)

Figure 1. (A) Schematic Configuration of Josephson Junction Device
(B) Its Current-Voltage Characteristics

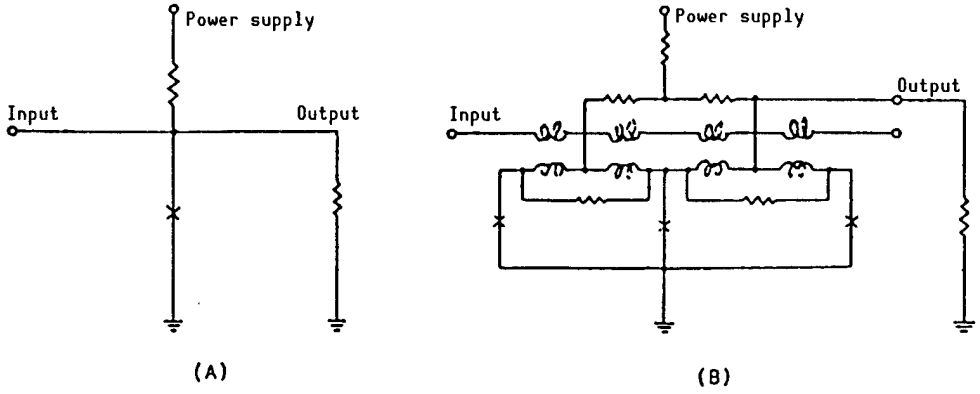


Figure 2. (A) Conceptual Drawing of Josephson Junction Switching Gate
(B) SQUID Josephson Gate With Input/Output Separation Function
("x" indicates Josephson junction devices)

Thus, power consumed by Josephson junction devices amounts to about one-thousandth of that consumed by semiconductors.

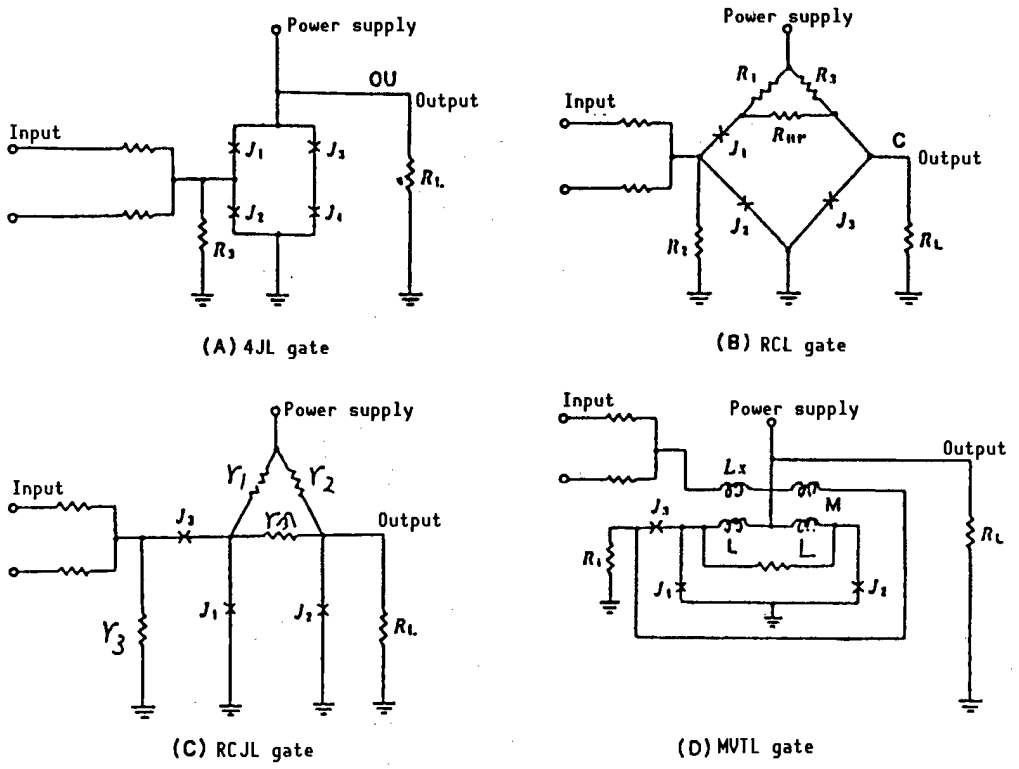


Figure 3. Current Injection Josephson Switching Gate

Josephson junction devices are two-terminal devices with two electrodes. Composing logic circuits by using the two-terminal devices as switching gates makes it difficult to separate input signals from output signals. This composition of logic circuits cannot be applied to integrated circuits. To resolve this problem, research was conducted on logic gates provided with functions to separate input signals from output signals by combining several Josephson junction devices with each other. Figures 2(A) and (B) show a conceptual drawing of a Josephson switching gate and a switching gate called "superconducting quantum interference device (SQUID) type" (development of which was promoted mainly by IBM in the United States), respectively.

SQUID switching gates are activated by the magnetic field induced by input signals. Meanwhile, an electric current is directly injected into Josephson junction devices to operate the switching gates. This is called an "electric current injection switching gate." Bell Research Institute in the United States first proposed electric current injection switching gates in 1979. In the same year, Electronic Research Institute developed for junction logic (4JL) gates composed of four Josephson junction devices. Later, research on Josephson integrated circuits using 4JL gates was promoted mainly in Japan. Figure 3 shows Josephson switching gates--being used mainly in Japan--developed by Electronic Research Institute, NTT, NEC Corp., Fujitsu Ltd., etc.

Table 1. Josephson IC Logic Circuit R&D Status

	Function	Operating time (clock frequency)	Gate speed (ps/gate)	Degree of integration (gate)
Kosaka, et al. (ETL, 1983)	Multiplier (4 x 4)	1,000		652
Nakagawa, et al. (ETL, 1985)	Shift register (4 bits)	195	15	74
Nakagawa, et al. (ETL, 1986)	ALU (2 bits)	157	13	174
Nakagawa, et al. (ETL, 1986)	Data processor (3 bits)	315	15	103
Kotani, et al. (ETL, 1987)	Multiplexer (4 bits)	1,050	11.5	900
Hatano, et al. (Hitachi, 1987)	Counter (4 bits)	650		
Nakagawa, et al. (ETL, 1987)	ALU (16 bits)	210	15	74
Kotani, et al. (Fujitsu, 1988)	Processor (4 bits)	770 MHz		1,841
Nakagawa, et al. (ETL, 1989)	Processor (4 bits)	705	15	1,866
Kotani, et al. (Fujitsu, 1989)	Processor (4 bits)	1100 MHz	15	3,056
Hatano, et al. (Hitachi, 1989)	Processor (4 bits)	1020 MHz		2,066
Nakagawa, et al. (ETL, 1989)	Computer (4 bits)	1,000	15	3,658
Hatano, et al. (Hitachi, 1990)	Processor (4 bits)	1000 MHz	20	3,665
Kotani, et al. (Fujitsu, 1990)	OSP (8 bits)	1000 MHz		6,300

Devising the circuit for these Josephson switching gates makes it possible to form logic gates that carry out logical add, logical multiplication, and logical negation. Further, combining these logic gates with each other permits optional logic circuits for large-scale integrated circuits to be formed. R&D on Josephson logic circuits has made marked progress, coupled with the development of Nb-based Josephson integration technology. As presented in Table 1, various logic integrated circuits and processors were manufactured on a trial basis. Processor operation experiments that emphasize the verification of high-speed operations have confirmed that the processor operated at ultrahigh speed with partial circuits.

Both logic and memory circuits play vital roles in the composition of Josephson computers. A persistent current, which is peculiar to the superconducting phenomenon, is used for the memory cells, which record information, of the memory circuit. The persistent current is induced in the closed loops of the superconducting lines that contain Josephson junction devices. These closed loops are used as information units. Even if the power supply is stopped, information continues to be stored by the persistent current. Memory cells using a persistent current that is equivalent to magnetic flux quantum are superior in low-power consumption and high-speed processing as is the case with logic circuits. Therefore, LSI memory chips that have integrated memory cells have been developed. Figure 4(A) shows a memory cell for Josephson random access memory (RAM), developed by IBM, and (B), (C), and (D) show the circuit diagrams of memory cells being developed.

Memory cells (B), (C), and (D), which are under development, possess the following features:

(B) Variable-threshold-memory cell:

Small, high-speed memory cells with a wide operation allowance have been developed by removing sense gates (used to detect persistent current in memory cells) from cells.

(C) Flux-quantum-transition memory cell:

Each gate for writing, located inside closed loops of persistent current flows, is composed of a single Josephson junction device.

(D) Capacitive-coupling-memory cell:

Each sense gate is composed of a single Josephson junction device connected to memory loops with capacitance.

The capacity of these memory cells ranges from 1~4 kilobits. These memory cells are integrated on a chip--together with memory-cell-driving circuits using Josephson switching gates as shown in Figure 2--so that access for random writing and reading can be carried out as RAM chips. Table 2 presents information on the R&D of Josephson RAM chips.

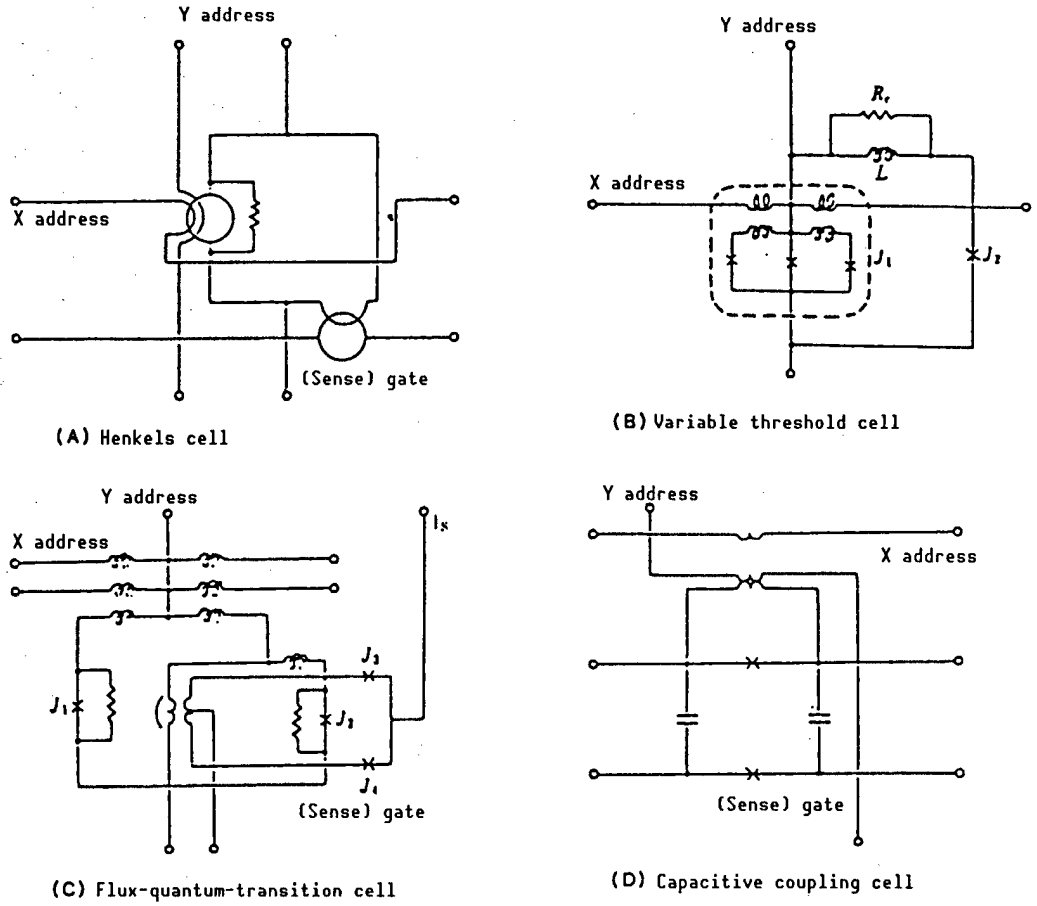


Figure 4. Equalizing Circuit for 1-Bit Memory Cell for Josephson RAM: A pair of X and Y address current designates the memory cell address, thus causing access operation.

With respect to variable-threshold-memory cells, Electronic General Research Institute has confirmed the possibility of properly accessing all 1,024 bit cells without providing redundant bits. This is a large breakthrough in the difficult development of Josephson memory RAMs.

On the basis of the above circuit technology, General Electronic Research Institute designed a Josephson ETL-JCI computer by integrating the technologies for logic circuits, the memory circuits, and the integration process and manufactured an ETL-JCI composed of four Josephson LSIs. The Institute has confirmed that a 128-step instruction program can be run and has thus succeeded for the first time in verifying Josephson computer operation functions.

Table 2. Josephson Memory R&D Status

	Memory cell	Storage capacity (bits)	Access time (ps)	Power consumption (mW)	Access operation
Henkels, et al. (IBM, 1983)	Henkels	1 K	700		
Yamamoto, et al. (NTT, 1983)	Henkels	1 K	3,500	2.0	Several bits
Wada, et al. (NEC, 1988)	Henkels	1 K	570	6.0	40%
Kurosawa, et al. (ETL, 1988)	Variable threshold	1 K	500	1.9	98%
Suzuki, et al. (Fujitsu, 1988)	Capacitive coupling	4 K	590	19	
Yano, et al. (Hitachi, 1990)	Huffle	1 K	700	10	
Kurosawa, et al. (ETL, 1990)	Variable threshold	1 K	500	1.9	100%
Tahara, et al. (NEC, 1990)	Flux quantum transition	4 K	580	6.7	Several tens of bits

3. Josephson ETL-JCI Computer

To verify Josephson computer operation functions, it is necessary to concurrently develop logic circuits and memory circuits so that Josephson logic circuit chips and Josephson memory chips can be connected to each other. The Josephson ETL-JCI computer was designed to verify the operational principle of Josephson computers, which is a 4-bit (though small in size) computer with all functions indispensable for computer operation such as arithmetic logic operation, sequence control, conditional branch, internal program storing, and data memory. To design a computer system, we employed the reduced instruction set computer (RISC) architecture that executes one instruction at one clock cycle using the ultrahigh-speed characteristics of a Josephson junction device and the (Harvard) architecture in which the instruction program memory path line is separated from the data memory path line.

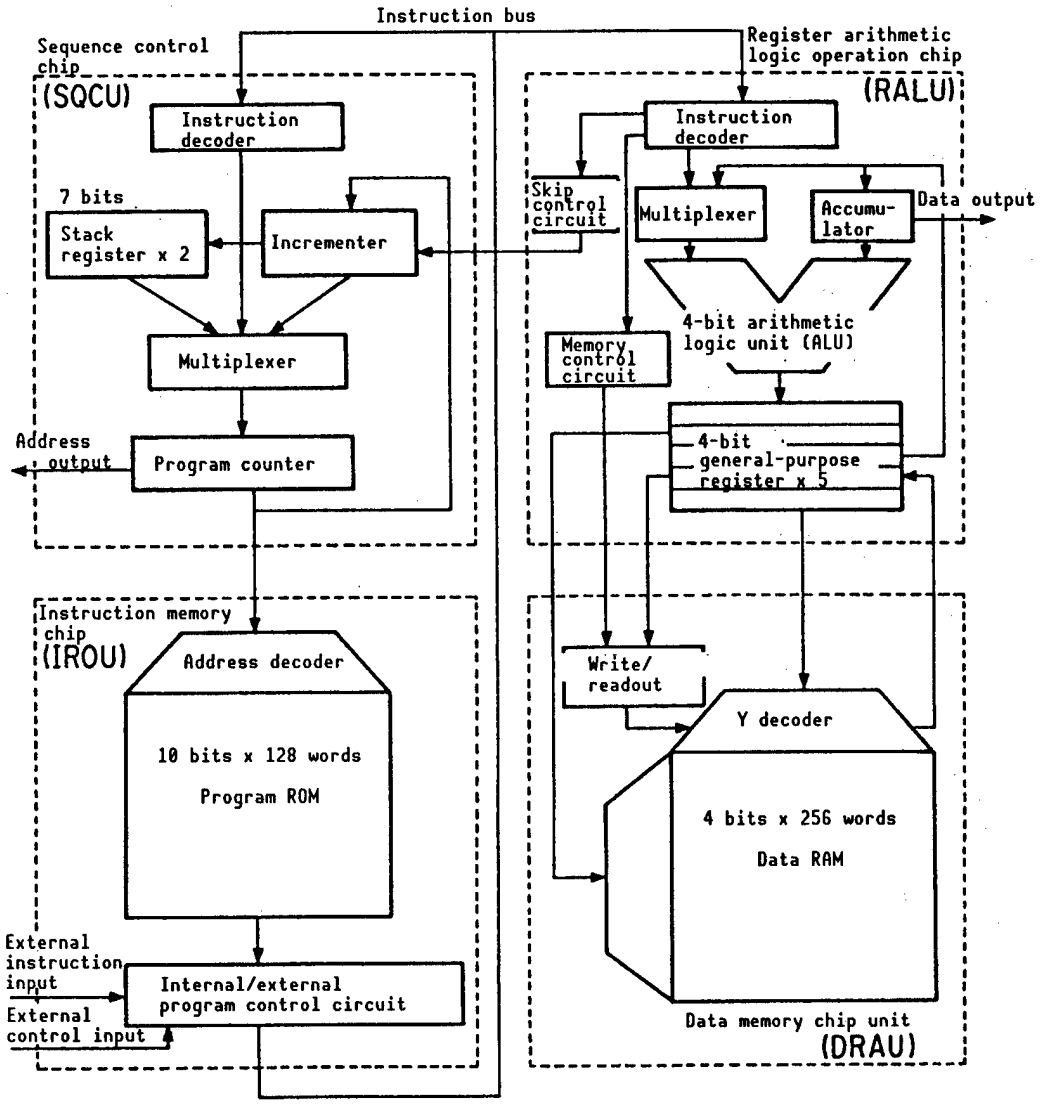
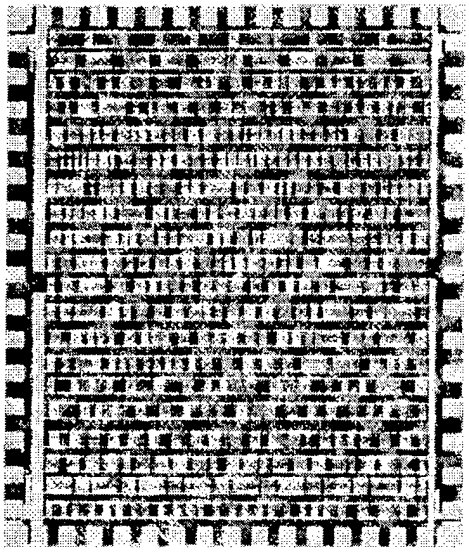
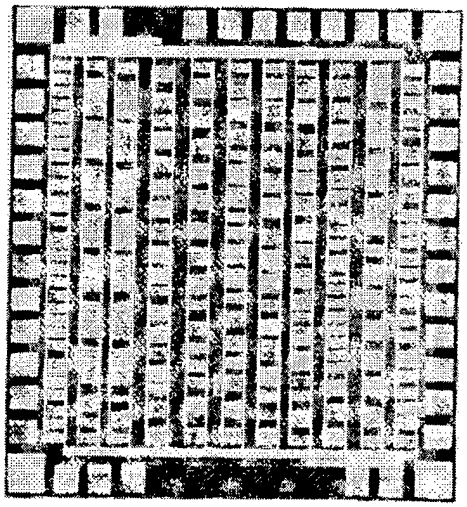


Figure 5. Josephson ETL-JCI Computer Program Block Diagram: 4-bit computer consisting of operation execution, sequence control, instruction program memory, and data memory based on RISC architecture.

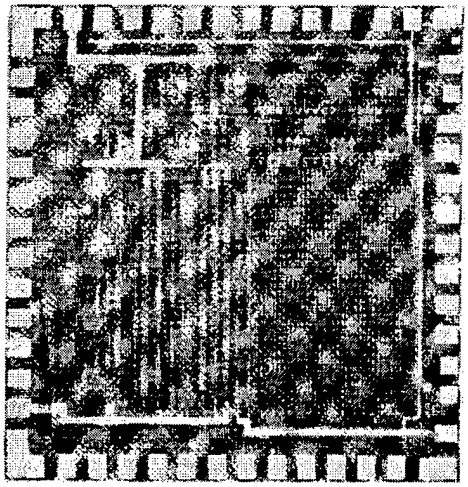
Figure 5 shows a block diagram on the Josephson ETL-JCI computer designed based on the said architectures. This computer has two logic circuit chips and two memory chips. In other words, it has four chips such as a register arithmetic logic unit (RLAU), sequence control unit (SQCU), instruction memory unit (IROU), and data memory unit (DRAU), and can compute and process 4-bit data. The capacity of the instruction memory and the data memory is 1,230 bits and 1,024 bits, respectively. The ETL-JCI computer runs a program stored in the read-only memory (ROM) of the IROU. The program has 27 instructions, including arithmetic logic operation, register control, writing into and reading from the data memory, unconditional/conditional branch, etc. By running this program, the ETL-JCI computer functions can be verified.



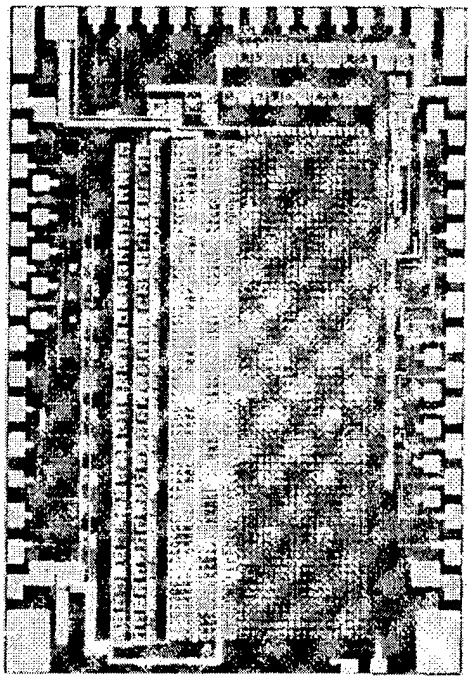
(A) Register arithmetic logic operation unit (RALU)



(B) Sequence control unit (SQCU)



(C) Data RAM unit (DRAU)



(D) Instruction ROM unit (IROU)

Figure 6. Josephson LSI Chips Comprising ETL-JCI Computer

The basic operation of the ETL-JCI computer is described below. First, the instruction codes of (one instruction = 10-bit length) the program stored in the instruction program memory chip are read out. These codes are sent to the register arithmetic logic unit chip and the sequence control chip via the instruction bus, and their contents are decoded by the decoder circuit. The register arithmetic-logic-operation chip carries out arithmetic or logic operation in accordance with the above instruction codes.

The results of operation are temporarily stored in the register. These data are written as necessary in the data memory (RAM) chip and read out. In the sequence control chip, the 7-bit address, in which instruction codes executed at the next clock cycle according to their contents are stored, is specified and sent to the instruction memory chip.

The ETL-JCI computer can execute program functions indispensable for computers such as conditional judgment and repetitive operation, using unconditional/ conditional branch and subroutine instructions.

To manufacture logic integrated circuit chips for the ETL-JCI computer, a computer aided design (CAD) system capable of precisely designing Josephson LSI chips rapidly was developed. Using this CAD system, logic simulations verified the correct design of the logic circuit. Along with this, the high-speed performance of the computer was evaluated and photomask patterns using the standard cell system were prepared. The four Josephson LSI circuits composing the ETL-JCI computer using niobium metal superconductors and 3-micron design rules were prepared. Figure 6 shows these four Josephson LSI chip photographs, (A) arithmetic logic operation chip (4.3 mm x 5.0 mm); (B) sequence control chip (3.0 mm x 3.2 mm); (C) instruction memory chip (3.75 mm x 5.0 mm); and (D) data memory chip (3.7 mm x 3.8 mm). About 22,000 Josephson junction devices are integrated on these LSI chips, forming logic circuits and memories.

All the circuits of the above chips were proven to operate normally. Then these chips were mounted on a computer wiring board, and wires were connected as shown in Figure 7. Thus, the ETL-JCI computer was composed.

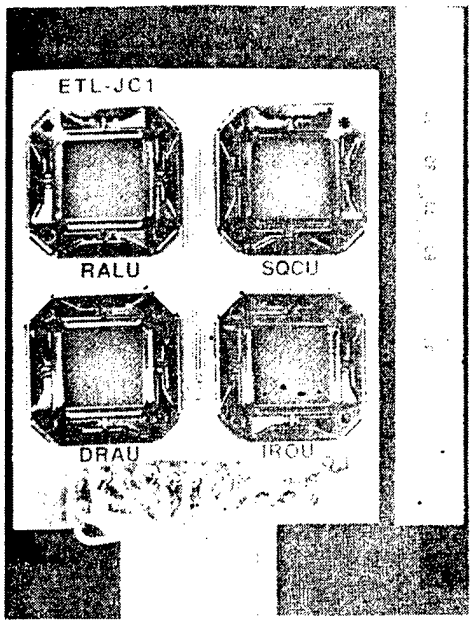


Figure 7. Josephson ETL-JCI Computer. Four Josephson LSI chips were put on a nonmagnetic chip carrier using bonding wiring. Then each chip carrier was connected to the wiring board. Signal output/input uses a coaxial cable, and power is also supplied using a coaxial cable

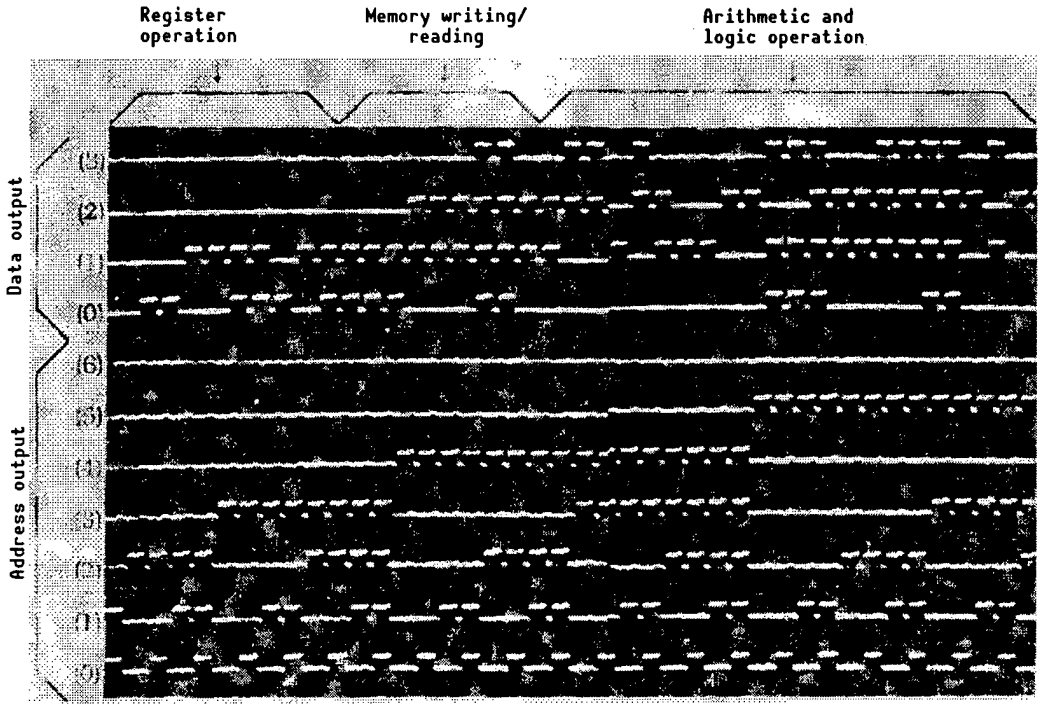


Figure 8. Josephson ETL-JCI Computer Operation Waveform: Operation waveforms when the instruction program stored in the internal memory ROM was executed. The upper 4-bit oscillograph waveforms are signals output from the accumulator and show the results of arithmetic and logic operations, etc. The lower 7-bit oscillograph waveforms show instruction program execution addresses. These operation waveforms have confirmed that the ETL-JCI computer properly carries out operations in accordance with the program.

On both sides of the wiring board, wiring to connect individual chips to each other used strip lines. All wiring boards were manufactured using nonmagnetic materials to avoid magnetic effects operating on the Josephson integrated circuit. Further, to prevent malfunction because of external magnetic fields such as a geomagnetic field, the ETL-JCI computer was covered by a magnetic shield and put in a liquid helium container. Thus, performance was tested.

The ETL-JCI computer begins operation after the designated (from outside) activation address of the program stored in the instruction program memory chip is activated. Actually, data temporarily stored in all registers, accumulators, and carry flags had been initialized via the external control circuit before the program activation address was designated. During the execution of the 128-step instruction program, the 7-bit program address and 4-bit accumulator data showing the results of arithmetic operation were read on all oscilloscopes and compared with the results of logic simulation carried out during circuit design. As a result, operational tests have confirmed that computer operations such as register control, writing into and reading from the memory, and arithmetic logic function can be properly executed in accordance with the program instructions stored in the computer. Figure 8 shows an example of the operation waveform during the execution of the program.

The computer, however, operates at low speed because of improper packaging technology, which allows structure signals to be transmitted and received between chips, preventing the high-speed driving of the power supply as shown in Figure 7. The results of delay time measurements and logic circuit simulations, however, show that data signals propagate at ultrahigh-speed in each chip. In addition, complicated operations were verified such as conditional-branch instruction, repetitive operation, and subroutine call/return that computers require. A total power consumption of 6.2 mW (about one-thousandth the power consumption of a semiconductor) was needed for the 22,000 Josephson junction devices of the ETL-JCI computer to be operated during the execution of the said programs. This power consumption has revealed that computers using Josephson junction devices operate with extremely little energy. If signal delay--arising from long wiring between chips--is removed from the results of measurement of the delay time of logic gates (used for ETL-JCI computer) and memory access time, one instruction is calculated to be executed in 1 nanosecond (one-billionth of a second) or less. Given that such high-speed logic operations can be carried out by a central processing unit (CPU), higher performance can be expected from Josephson computers by introducing advanced software (already developed) such as parallel processing. The major performance specifications of the ETL-JCI computer are as given in Table 3. Electricity required to operate Josephson junction devices is almost constant irrespective of clock frequency.

4. Future Problems

The operational principle of Josephson computers has been revealed, and research on Josephson computers has begun to at last take shape. Many technological subjects, however, require study in the future, including the power supply for the Josephson junction drive. Because of their operational principles, Josephson junction devices are operated on an ac power supply. Therefore, if Josephson logic circuits were given tens of thousands to hundreds of thousands of gates driven by a frequency of 1 GHz, they would require considerable changes in technology. To what density can Josephson memory RAMs be integrated is also a major subject. Design conditions are such that they can capture magnetic flux quantum and thereby induce persistent current to which the simple scaling rule cannot be applied. The development of a packaging technology is indispensable, because it would allow the mounting of a large number of Josephson LSI chips in order to transmit and receive ultrahigh-speed signals between chips. Nonmagnetic chip mounting boards must be developed to withstand the cryogenic environments of liquid helium. If Josephson computers are completed, they will be placed in a cryogenic atmosphere of liquid helium. It is necessary, therefore, that a method of effectively connecting input/output units maintained at room temperature or Josephson computers to the peripheral equipment must also be developed. To fully utilize the high-speed performance of Josephson computers, interfacing must be properly done.

Table 3. Characteristics of Josephson ETL-JCI Computer

Item	Details
Josephson junction device	Niobium/aluminum oxide/niobium (3 μm design rule)
Basic circuit	4JL gate family (for logic), variable-threshold-memory cell (for RAM), 2 junction SQUID cell (for ROM), directly coupled latch (for temporary storing)
Chip composition (4 chips)	Register arithmetic, logic operation (RALU) chip: 1,273 gates, 4.3 x 5.0 mm Sequence control (SQCU) chip: 593 gates, 3.0 x 3.2 mm Instruction memory (IROU) chip: 10 bits x 128 words, 4.5 x 5.0 mm Data memory (DRAU) chip: 4 bits x 256 words, 3.7 x 3.8 mm
Instruction structure	10 bit length x 27 types: Arithmetic, logic operation, shift operation, unconditional/conditional branch, data transmission, memory control, subroutine call/return
Data and address structure	Data: 4-bit length; instruction address: 7-bit length; data memory address: 8-bit length
Architecture	RISC (reduced instruction set computer) architecture, (Harvard) (instruction memory/data memory branch) architecture
Input/output	External instruction input, external control input/data output, address output
Drive system	Two-phase pulsation power supply
Execution of operation	1 instruction/1 clock cycle
Design	Use of Josephson LSI logic CAD based on standard cell
Operation time	1 ns/1 instruction (logic simulation)
Power consumption (4-chip total)	6.2 mW (including regulator)

5. Oxide Superconductor

Completely new electronic material, called a "high-temperature oxide superconductor," was discovered in 1986, and R&D on this new material is being conducted worldwide. This is good news for the development of Josephson computers. Research seeks to apply high-temperature oxide superconductors to the electronic field, as well as to make clear the mechanism and to further explore new superconducting materials. Such electronic fields include Josephson junction devices that use high-temperature oxide-superconductors as electrodes and a new electronic device called a "three-terminal device." The author noted that high-temperature oxide superconductors possess high-critical

temperatures that cannot be estimated from metal superconductors. High-temperature oxide superconductors whose critical temperatures exceed 110 K have already been discovered. If high-speed signals can be transmitted and received on superconducting microstrip lines at temperatures ranging from 4.2 K to 72 K (liquid nitrogen), it will become possible to effectively connect CMOS and HEMT transistors (operating at 77 K) to Josephson junction devices. This appears to be the first step toward solving the abovementioned fourth subject. The application of high-temperature oxide superconductors to the electronic field as were semiconductors is desirable.

6. Conclusion

The author described the course of research on Josephson integrated circuits, an outline of research on the world's first Josephson ETL-JCI computer, and the future tasks and outlook for the development of Josephson computers. The Josephson junction devices to date developed are two-terminal ones and have had difficulty composing computer circuits. This technological problem, however, has probably been solved through the performance test of the ETL-JCI computer. It has been revealed that 22,000 Josephson junction devices can be operated as a system using only 6 mW of electric power. On the basis of this discovery, research must be conducted on the higher integration of Josephson integrated circuits; high-speed cryogenic packaging technology; and the peripheral technology so that the ultrahigh-speed performance of Josephson junction devices can be demonstrated. In the future, heat generation from the use of large-sized computers will be resolved. In addition, the next-generation supercomputers will be developed using Josephson junction devices. Great hopes are placed on these points.

References

1. Sugano and Hayakawa, "Ultrahigh-Speed Josephson Device," Baifukan, 1986.

2. Nakagawa, et al., Extended Abstracts of ISEC 89, Tokyo, 1989.

3. Kotani, et al., Ibid.

4. Hatano, et al., Ibid.

5. Nakagawa, et al., Electronic Information Communications Society Technical Report, SCE 89-59.

6. Kotani, et al., Electronic Information Communications Society All-Japan Spring Meeting, preliminary lecture draft 5-351, 1990.

7. Suzuki, H., et al., IEEE TRANS. MAGN., Vol 25, 1989, p 783.

8. Yano, et al., Electronic Information Communications Society Technical Report, SCE 89-59, 1990, p 55.

9. Kurosawa, et al., 1990 Symposium on VLSI Circuits, Honolulu, 1990.

10. Tabara, et al., Electronic Information Communications Society IC Research Society, Tsukuba, June 1990.

11. Kitazawa and Ishiguro (ETS), Advances in Superconductivity, Proceedings of First International Symposium on Superconductivity (ISS 88), Nagoya, Springer-Verlag, 1988.

YBCO Film Fabrication by MOCVD Method

916C0001B Tokyo TOKAI CHIKU KO ON CHODENDO KENKYU HAPPYOKAI in Japanese
17 Jul 90 pp 16-17

[Article by H. Hiki, M. Umeno, M. Maeda, and A. Suzuki, Nagoya Technical College; and N. Ushida and K. Higashiyama, Superconducting Engineering Research Institute]

[Text] **1. Preface**

The preparation of thin film oxide superconductors is being studied using many processes. The metallo-organic chemical vapor deposition (MOCVD) process used to prepare semiconductor thin films is superior in controlling composition and transferring mass production to other film preparation processes. This process, therefore, is being studied by many research laboratories as one of the superconducting thin film preparation technologies. Problems with the deterioration of raw materials, etc., however, prevent taking complete advantage of good control of composition. The author, et al., therefore, improved the control of composition using equipment, observed heterogeneous phases that precipitate when the film composition ratio deviates from 1:2:3 (Y:Ba:Cu), and studied the effect of heterogeneous phases on the characteristics and orientation of YBCO with respect to the preparation of Y group superconducting thin films.

2. Experiments

Two types of MOCVD equipment were used. In the first type, the gasoline that connects the raw material vessel to the reaction tube was insulated from heat by winding heaters. In the second type, the gasoline was installed in a hot-air-circulation, constant-temperature bath. Figure 1 shows a schematic drawing of the second type. Table 1 also presents the film preparation conditions. Substrates were heated by ceramic heaters and cooled in atmospheric O_2 after film formation. The film compositions were measured by ICP and EDX.

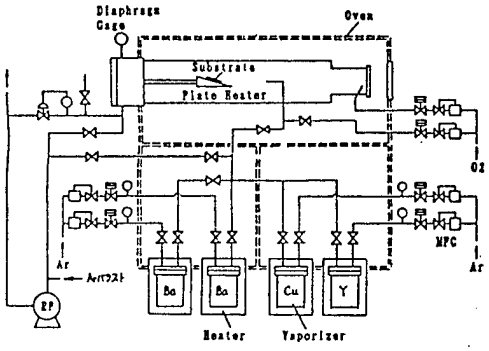


Figure 1. MOCVD Equipment

Table 1. Film Preparation Conditions (Example)

Substrate: Heating temperature		HgO (100)	650~750°C
Raw material: Heating temperature		$Y(DPM)_3$	125°C
		$Ba(DPM)_2$	233~238°
		$Cu(DPM)_2$	118~120°C
Furnace pressure:	10 Torr		
Film preparation time:	1 hour		
Carrier gas:	Ar		
Film thickness:	~1 μ		

3. Results and Study

3.1 Dependence of Equipment on Controlling Composition and Raw Material Stable Supply Performance

How the control of the composition and the raw material stable supply performance changed was investigated by using a constant temperature bath (as mentioned above) to heat the gasoline in the equipment. The two types of equipment were compared with respect to controlling the composition in terms of the film composition ratio C_{Cu}/C_{Ba}. As a result, controlling the composition varied within a range of about ±30 percent in type I (resistance A heating system); whereas, it varied within a range of about ±10 percent in type II (constant-temperature bath). We paid attention to Ba raw material, which is heated at high temperatures and deteriorates at the fastest speed. In type I, the raw material (solid at room temperature: 5 g) was replaced with new material every 25 hours in terms of aggregate film preparation time; whereas, in type II, the raw material was able to be stably used for about 80 hours. this is because the decomposition and solidification of raw gas, which is caused by temperature distribution in the gasoline, decreased. Loss in the gas line decreased, and the raw material was maintained at slightly lower temperatures. As a result, the raw material was able to be stably used for about 80 hours.

3.2 Composition Ratio and Heterogeneous Phase

Films (prepared at 830~850°C) whose composition ratio is nearly 1:2:3 and those whose composition ratio slightly deviates from 1:2:3 were studied. Then, the type and shape of heterogeneous phases that precipitated from the respective films was investigated. As a result, we have found that the following crystals precipitated as heterogeneous phases:

(1) From Y-rich region: needle-shaped crystal Y_2BaCuO_5
(2) From Y-poor, Ba-rich region: square crystal $BaCuO_2$
(3) From Cu-poor, Ba-rich region: round crystal YBa_3Cu_2Ox
(4) From Cu-rich region: spherical crystal CuO

In Y_2BaCuO_5 phases, crystals were observed to grow in the shape of needles between YBCO phases and to interfere with the growth of YBCO phases. In addition, the Tc (Ac magnetization rate measured Tc) of each film was measured by the four-probe method. The Tc of the films having a composition ratio of 1:2:3 was 79 K (72 K). The Tc of the films, from which heterogeneous phases precipitated, was 1) 62 K (68 K), 2) 65 K (61 K), 3) 65 K (60 K), and 4) 78 K (75 K), respectively. In other words, Tc was lowered when the composition ratio deviated from 1:2:3. The deterioration of Tc characteristics, however, was not observed solely when CuO phases precipitated. Because CuO that precipitates due to excessive Cu composition appears in the spherical form on YBCO without combining with other component elements (Y, Ba), it does not greatly prevent the growth of YBCO as is the case with Y_2BaCuO_5.

3.3 Effect of Excessive Cu Composition on YBCO

On the basis of the results set forth in 3.2, the effect of excessive Cu composition on YBCO phase was using type II equipment. Figure 2 shows SEM images and XDR results of films (prepared at 700°C) having a composition ratio of (a) 1:2:3, and (b) 1:2:3.6, respectively.

According to the results of XDR (a), (110), (103) peak is slightly more apparent than the c-axis oriented peak. The results of XRD (b) show that c-axis orientation grows in the YBCO phase, though the scanning electron microscope (SEM) image shows the presence of CuO grains. In addition, (b) shows an improved Tc compared with (a). We prepared several identical specimens and paid attention to (005), (200), (110) peak based on the results of XRD and plotted the strength ratio I(110)/I(005), I(200)/I(005) with respect to "x" of 1:2:x (Y:Ba:Cu). The results are as shown in Figure 3. The figure shows that, as the composition ratio of Cu increases, I(II0)/I(005) decreases and Tc is improved. These results show that excessive Cu causes the c-axis orientation of YBCO to grow. When films were prepared at 650°C, such a trend was clearly observed. It can be said, therefore, that when films are prepared at low temperatures, an excessive Cu composition greatly serves to improve the quality of YBCO.

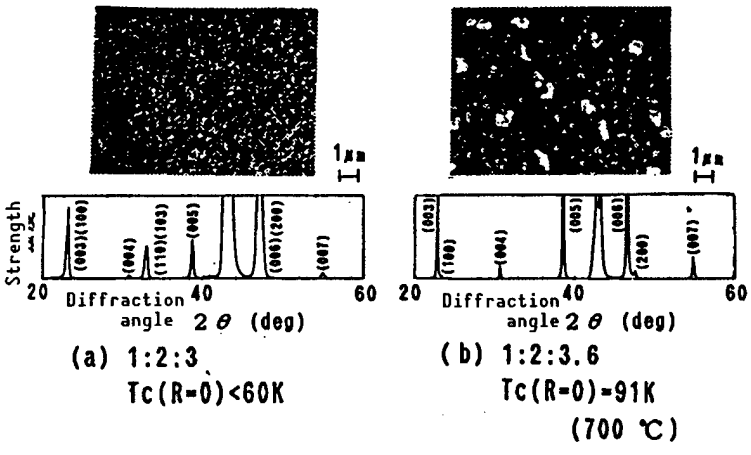


Figure 2. Effect of CuO Phase on YBCO (700°C)

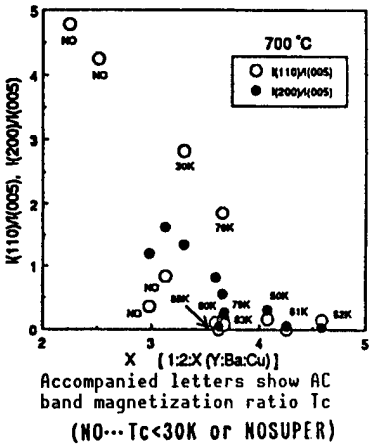


Figure 3. Excessive Cu and Orientation

4. Conclusions

• The heating of the gasoline in a constant temperature bath has made it possible to improve control of the film composition and the supply of stable raw material.

• Where YBCO phases contain heterogeneous phases, their superconducting characteristics generally deteriorate. The characteristics of only films containing CuO phases that precipitate due to excessive Cu composition, are slightly improved. Moreover, excessive Cu composition strengthens the c-axis orientation of YBCO.

Y-Based Superconductor Synthesis by Laser Process

916C0001C Tokyo TOKAI CHIKU KO ON CHODENDO KENKYU HAPPYOKAI in Japanese
17 Jul 90 pp 24-25

[Article by S. Nagaya, M. Miyajima, and I. Hirabayashi, ISTEC-SRL Nagoya Research Laboratory]

[Text] **Preface**

Orientation control, grain boundary reformation, and pinning are necessary to greatly improve Jc of oxide superconductors. As a process capable of carrying out orientation control and grain boundary reformation, for bulk materials, the melting process is being studied as a way to control orientation and reform grain boundaries.

In the case of Y group superconductors, 12 superconducting phases do not directly crystallize from the liquid phases, but Y_2O_3 and 211 phases, which are stable at high temperatures, are formed. Therefore, 123 phases are synthesized in the reaction form of 211, 123 using peritectic reactions in the partial melting region.

Peritectic reactions, however, are slow, involving diffusion in solid phases under interface local equilibrium conditions, and require very slow cooling speeds, that is, several degrees Centigrade per hour. When reactions cause crystals to grow at super high speeds, i.e., under quasi-stable condition, in which the solid-liquid interface moving rate (R) is large, the peritectic reactions are controlled. As a result, 123 phases are likely to be crystallized, as the first crystal, when the 123 composition becomes melted liquid because of the excessive cooling of the interface. To enable crystals to grow under quasi-stable conditions, a large temperature gradient (G) is more advantageous. By applying laser zone heating, the author, et al., therefore, tried the melt and rapid solidification method that can concurrently give a large temperature gradient and migration rate.

Method of Experiment: As samples, to which laser beams are irradiated, $YBa_2Cu_3O_x$ sintered pellets prepared by the general solid phase reaction process were used. As laser for heating, the continuous-wave Nd:YAG laser was used.

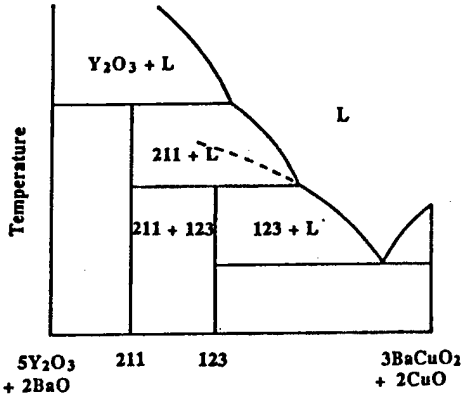


Figure 1. A pseudobinary phase diagram for the Y-Ba-Cu-O system which is a section through a ternary phase diagram along the tie line between the 211 and 123 phases.

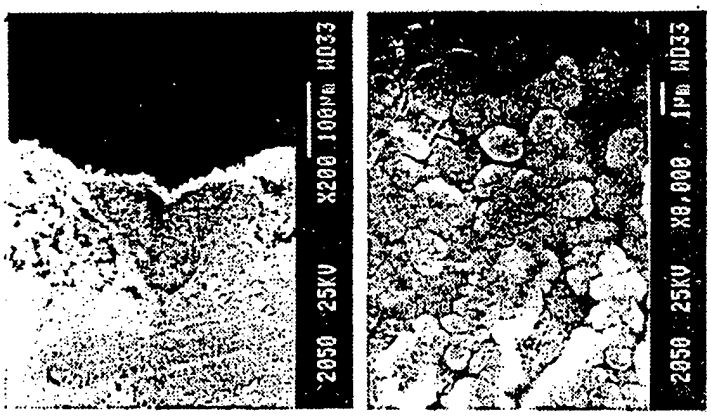


Figure 2. SEM micrograph of the polished cross section of a laser process sample.

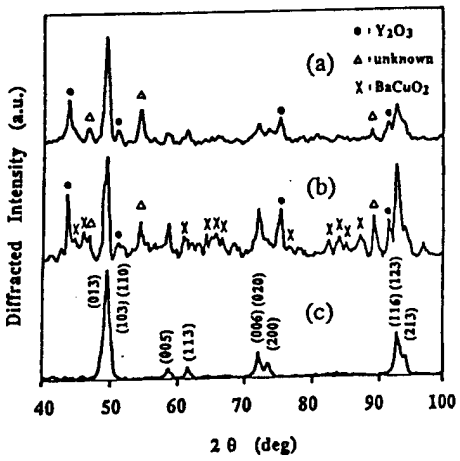


Figure 3. Micro-X-ray diffraction patterns and phase identification showing the main peaks of the 123 phase and others: (a) the cross section and (b) the surface of a laser process sample and (c) the nonirradiated original sample.

Results of Experiments: Figures 1 and 2 show a scanning electron microscope (SEM) micrograph of a cross section of the melted solidified portion and the results of XRD measurement of microscopic portions at a laser output of 100 W and a scan speed of 20 cm/second. The micrograph shows that a Dendlight-shaped structure was formed and that rapid solidification was accompanied by excessive interface cooling.

The results of the XRD measurement of microscopic portions show that the melted solidified portion comprises a multiphase, i.e., 123 phase and Y_2O_3, and that no 211 phases, which are usually formed by melting and solidification, were observed.

In this case, the following two reactions are believed to form the 123 phase.

$$L \rightarrow Y_2O_3 + L \rightarrow 123 \quad (1)$$

$$L \rightarrow 123 \quad (2)$$

Figure 3 shows the formation rates of 123 phases and Y_2O_3 at laser outputs of 50 W and 100 W, respectively, according to the scan speed.

As the scan speed--i.e., "R"--increases, the 123 phase increases and Y_2O_3 decreases. In the region where the crystal growth rate is slower (region where diffusion in the solid phase is large = region where peritectic reactions is more advance), Y_2O_3 increases.

This shows that the formation of the 123 phase is neither a two-stage peritectic reaction ($Y_2O_3 + L \rightarrow 211 + L \rightarrow 123$) so far thought nor a one-stage peritectic reaction set forth in (1) above; thus, the 123 phase was crystallized from the melted liquid of the 123 composition.

The rapid solidification depends greatly on the temperature gradient (G) of the solid-liquid interface and the crystal growth rate, i.e., the migration rate (R), of the solid-liquid interface. The migration rate can be controlled by the scan speed while the temperature gradient can be controlled by changing the profile of laser beams.

When laser beams of 50 W were irradiated, the melting zone width was reduced by half without changing the energy density, compared with the irradiation of laser beams of 100 W. (In this case, the melt depth was the same.) In other words, the temperature gradient was doubled. At the same scan speed, when laser beams of 50 W were irradiated, the 123 phase was formed about twice as fast as the irradiation of laser beams of 100 W. At the same amount of 123 phase formation, when laser beams of 50 W were irradiated, the scan speed was half that of laser beams of 100 W. This shows that the process corresponds to the cooling rate represented by the product of G and R.

As a result of XDR, the (013)/(103), (020)/(200), (123)/(213) peak separation --showing the presence of the ortho phase (superconducting phase) of the 123 phase--was observed. Measurements using a DC-SQUID have confirmed that the ortho phase has become a superconductor whose Tc = 94 K.

It is also possible to achieve rapid solidification equivalent to or higher than general quenching by high-speed crystal growth under a high-temperature gradient. Further, it is possible to microscopically disperse Y_2O_3 into the melted, solidified portion by controlling the irradiation conditions. In this case, it is possible to synthesize, by annealing, 123 phases at the general two-stage peritectic reaction ($Y_2O_3 + L \rightarrow 211 + L \rightarrow 123$). We also succeeded in synthesizing samples with $Jc = 1 \times 10^4$ (A/cm^2) or larger, though estimated, by leaving the 211 phase, that is, the reaction residue.

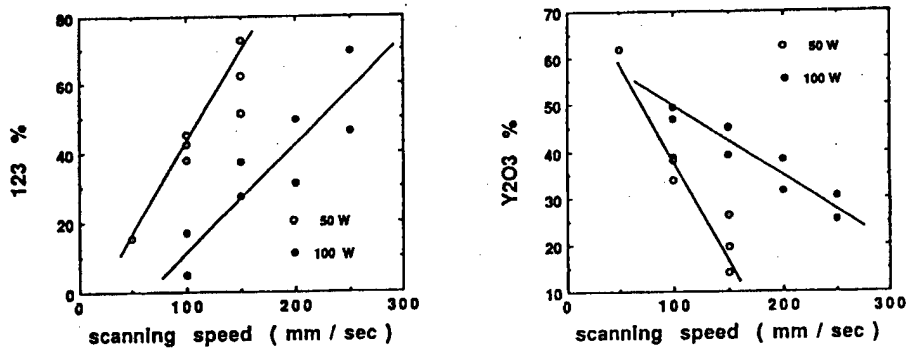


Figure 4. Phase fraction estimated from the intensity of the total 123 phase peak intensity and the total Y_2O_3 phase peak intensity against the total peak intensity from 40~100 degrees of 2 θ versus a scanning velocity of 50 W and 100 W.

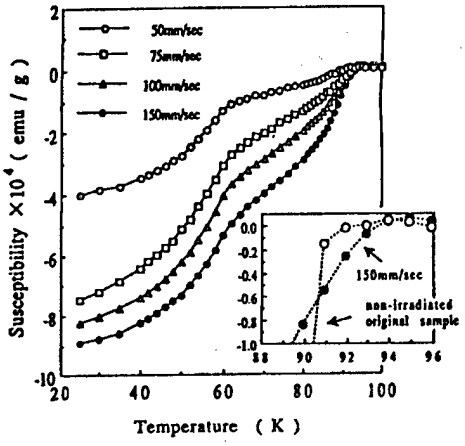


Figure 5. Temperature dependence of the field cooled susceptibility (50 Oe) of laser process samples with 50 W.

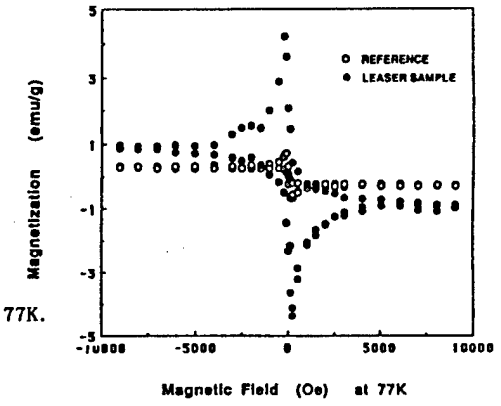


Figure 6. Magnetization loops for the laser process annealed sample at 75 K.

Production of High Electric Current Density

916C0001D Tokyo TOKAI CHIKU KO ON CHODENDO KENKYU HAPPYOKAI in Japanese
17 Jul 90 pp 44-45

[Article by K. Hayashi and A. Yada, Toyohashi Technical College; K. Ohba, Topy Industrial Co., Ltd.; A. Ohta, Daiichi Technical Research Institute]

[Text] **1. Preface**

Of various approaches to manufacture wires using high-temperature oxide superconductors, the metal sheath processing method is thought to be most suited to manufacturing lengthy wires. In this process, superconducting oxide powder is first sealed in a metal sheath (pipe). Then, the metal sheath is drawn, rolled, and sintered to manufacture a wire. Silver, which does not directly react to oxide, is used as sheath metal.

This research seeks to do the following two things, paying particular attention to Bi(Pb) based high-temperature oxide superconductors: 1) preparing Bi(Pb) based superconducting wires with a high Jc using the silver sheath processing method; and 2) studying magnetic flux creep by conducting experiments on the electromagnetic field characteristics of high Jc wires.

2. Method of Experiments

Sintered powder ($Bi_{1.6}Pb_{0.4}Sr_{2.0}Ca_{2.2}Cu_{3.2}O_x$) is sealed in a silver sheath and cold processed by grooved roll, producing a square thin wire (1 mm square) with a square cross section. The square thin wire is further cold processed by flat roll, producing a tape (thickness: 0.15 mm), and sintered (primary sintering) at 832°C (constant). The sintered wire is further cold rolled (one to three times), sintered (two to four times), and used as a specimen. The total sintering time is varied within a range of 60~260 hours. Figure 1 shows a cross section photograph of wire specimens with various thicknesses. The scanning electron microscope (SEM) image (Figure 2) of rupture surfaces of wire specimens and results of X-ray diffraction measurements show a microscopic structure with its c-axis oriented vertically to the tape surface. I-V characteristics of wire specimens are measured at 77K with the magnetic field at the parameters. Then, Jc at H = 0 and its magnetic field characteristics are investigated. Further, magnetization changes over time when magnetic

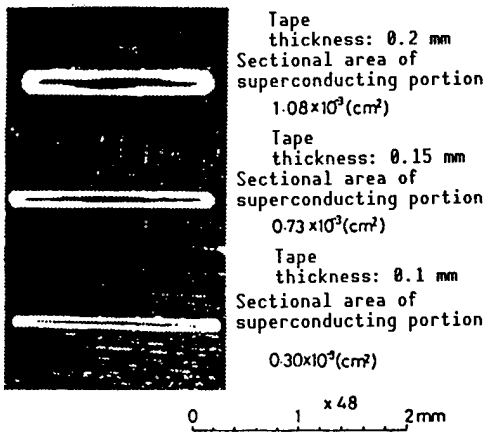


Figure 1. Cross-Section Photograph of Silver-Sheathed Tape

Figure 2. SEM Image of Tape Wire Ruptured Surface

fields of 500 Oe and 30 Oe are applied and when both ZFC (application to magnetic field after cooling) and FC (cooling after application of magnetic field) are measured using a SQUID.

3. Results of Experiments

When the sintered powder was used as a sealing powder, Jc was a maximum of 2,400 A/cm^2 at H = 0, which was inferior to that obtained when temporarily burnt powder was used. In addition, even when antimony was added, no high Jc was obtained. Figure 3 shows Jc versus the total sintering time. The optimum total time from second to fourth sintering is 50~70 hours. In particular, when the primary sintering time is 100 hours, a Jc was a maximum of 6,400 A/cm^2. When the primary sintering time is 100 hours or more, rolling two or more times is not effective.

The results of measurement of Jc in the magnetic field can be arranged as follows:

(1) Wires deteriorate markedly when a magnetic field is applied vertically (vertical magnetic field) to the tape surface than when parallel with the tape surface (parallel magnetic field) (Figure 4).

(2) The higher the Jc (H = 0) of the wire, the less the wire deteriorates.

(3) The thicker the wire, the less the wire deteriorates.

(4) Deterioration of wires does not depend on the preparation process (number of repeated rolling, sintering conditions, etc.).

Figure 4 shows Jc - H characteristics of a wire whose Jc = 6,300 A/cm^2 at H = 0. The figure shows that Jc's of 1,400 A/cm^2 and 670 A/cm^2 can be obtained in a parallel magnetic field (1 kOe) and a vertical magnetic field, respectively. In either case, Jc linearly decreases at 500 Oe or larger, together with the magnetic field (logarithm).

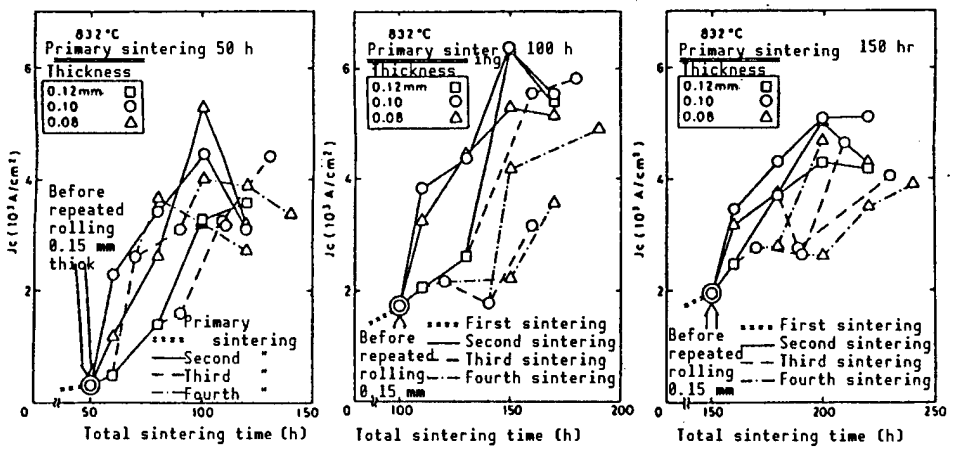


Figure 3. Sintering Time Dependence of Tape Wire Jc

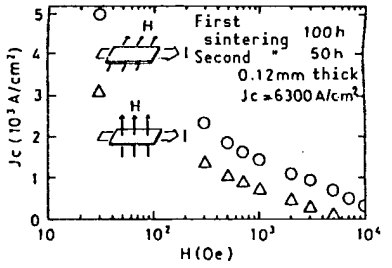


Figure 4. Jc–H Characteristics of Tape Wire

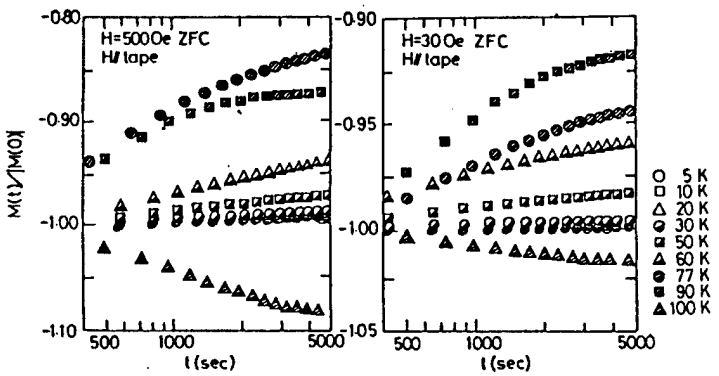


Figure 5. Changes in Magnetization of Tape Wire (due to passage of time)

Magnetization relaxation was measured for a wire of 0.1 mm in thickness, whose Jc is 5,400 A/cm^2 at H = 0. Magnetic fields of 500 Oe and 30 Oe were applied in parallel with the tape surface at temperatures ranging from 5~100 K in both ZFC and FC cases. Then, the passage of time changed magnetization which was measured using the Quantum Design Corporation's MPMS. The passage of time changed magnetization, which was measured by applying magnetic fields of 500 Oe and 30 Oe under ZFC. The results of measurements are shown in Figure 5.

At temperatures of 90 K or lower, diamagnetic susceptibility almost linearly decreases with respect to the logarithm (1 n t) of time. At 100 K, however, diamagnetic susceptibility increases. Figure 6 shows the gradients of magnetization of the logarithm (magnetization gradient) in both ZFC and FC cases.

When magnetic fields of 500 Oe and 30 Oe are applied under ZFC, the magnetization gradient is always positive and becomes larger from 5~10 K as the temperature rises. Magnetic flux movement (magnetic flux creep) appears to intensify because of thermal activity. When the temperature further rises, the

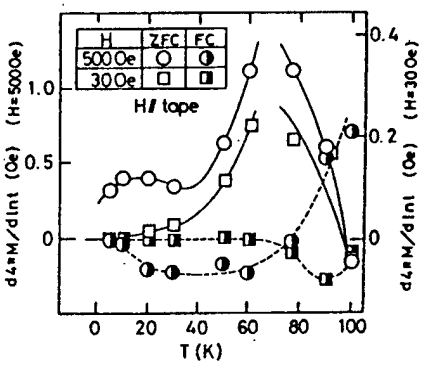


Figure 6. Temperature Dependence of Magnetization Gradient of Taper Wire

magnetization gradient shows a sharp peak, unlike the behavior of general magnetic flux creep. Thereafter, the magnetization gradient rapidly decreases. Where magnetic fields of 500 Oe and 30 Oe are applied under FC, the magnetization gradient has negative values at low temperatures (about 60 K or lower). When the temperature rises, again the magnetization gradient shows a small negative peak at about 90 K with the application of a magnetic field of 30 Oe. However, when a magnetic field of 500 Oe is applied, the magnetization gradient rapidly rises and becomes positive, and an abnormal behavior of magnetic flux creep behaves abnormally at the higher temperatures near Tc, as is the case with ZFC.

- END -

Foreign Broadcast Information Service (FBIS) and Joint Publications Research Service (JPRS) publications contain political, military, economic, environmental, and sociological news, commentary, and other information, as well as scientific and technical data and reports. All information has been obtained from foreign radio and television broadcasts, news agency transmissions, newspapers, books, and periodicals. Items generally are processed from the first or best available sources. It should not be inferred that they have been disseminated only in the medium, in the language, or to the area indicated. Items from foreign language sources are translated; those from English-language sources are transcribed. Except for excluding certain diacritics, FBIS renders personal and place-names in accordance with the romanization systems approved for U.S. Government publications by the U.S. Board of Geographic Names.

Headlines, editorial reports, and material enclosed in brackets [ ] are supplied by FBIS/JPRS. Processing indicators such as [Text] or [Excerpts] in the first line of each item indicate how the information was processed from the original. Unfamiliar names rendered phonetically are enclosed in parentheses. Words or names preceded by a question mark and enclosed in parentheses were not clear from the original source but have been supplied as appropriate to the context. Other unattributed parenthetical notes within the body of an item originate with the source. Times within items are as given by the source. Passages in boldface or italics are as published.

SUBSCRIPTION/PROCUREMENT INFORMATION

The FBIS DAILY REPORT contains current news and information and is published Monday through Friday in eight volumes: China, East Europe, Soviet Union, East Asia, Near East & South Asia, Sub-Saharan Africa, Latin America, and West Europe. Supplements to the DAILY REPORTs may also be available periodically and will be distributed to regular DAILY REPORT subscribers. JPRS publications, which include approximately 50 regional, worldwide, and topical reports, generally contain less time-sensitive information and are published periodically.

Current DAILY REPORTs and JPRS publications are listed in *Government Reports Announcements* issued semimonthly by the National Technical Information Service (NTIS), 5285 Port Royal Road, Springfield, Virginia 22161 and the *Monthly Catalog of U.S. Government Publications* issued by the Superintendent of Documents, U.S. Government Printing Office, Washington, D.C. 20402.

The public may subscribe to either hardcover or microfiche versions of the DAILY REPORTs and JPRS publications through NTIS at the above address or by calling (703) 487-4630. Subscription rates will be provided by NTIS upon request. Subscriptions are available outside the United States from NTIS or appointed foreign dealers. New subscribers should expect a 30-day delay in receipt of the first issue.

U.S. Government offices may obtain subscriptions to the DAILY REPORTs or JPRS publications (hardcover or microfiche) at no charge through their sponsoring organizations. For additional information or assistance, call FBIS, (202) 338-6735,or write to P.O. Box 2604, Washington, D.C. 20013. Department of Defense consumers are required to submit requests through appropriate command validation channels to DIA, RTS-2C, Washington, D.C. 20301. (Telephone: (202) 373-3771, Autovon: 243-3771.)

Back issues or single copies of the DAILY REPORTs and JPRS publications are not available. Both the DAILY REPORTs and the JPRS publications are on file for public reference at the Library of Congress and at many Federal Depository Libraries. Reference copies may also be seen at many public and university libraries throughout the United States.